

AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 10-11, 14, 22, 25-26, and 28 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An apparatus for performing cryptographic operations, comprising:
a cryptographic instruction, received by a ~~microprocessor~~ pipeline ~~microprocessor~~ as part of an ~~instruction flow~~ ~~application program~~ executing on said ~~microprocessor~~ pipeline ~~microprocessor~~, wherein said cryptographic instruction prescribes one of the cryptographic operations, and wherein said one of the cryptographic operations comprises:
a plurality of CFB block cryptographic operations performed on a corresponding plurality of input text blocks;
CFB mode logic, operatively coupled to said cryptographic instruction, configured to direct said ~~microprocessor~~ pipeline ~~microprocessor~~ to update pointer registers and intermediate results for each of said plurality of CFB block cryptographic operations; and
execution logic, operatively coupled to said CFB block pointer logic, configured to execute said one of the cryptographic operations.
2. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:
a CFB mode encryption operation, said CFB mode encryption operation comprising encryption of a plurality of plaintext blocks to generate a corresponding plurality of ciphertext blocks.

3. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:
a CFB mode decryption operation, said CFB mode decryption operation comprising decryption of a plurality of ciphertext blocks to generate a corresponding plurality of plaintext blocks.
4. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations is accomplished according to the Advanced Encryption Standard (AES) algorithm.
5. (Original) The apparatus as recited in claim 1, wherein said cryptographic instruction prescribes that cipher feedback mode to be employed in accomplishing said one of the cryptographic operations.
6. (Original) The apparatus as recited in claim 1, further comprising:
a bit, coupled to said execution logic, configured to indicate whether said one of the cryptographic operations has been interrupted by an interrupting event.
7. (Original) The apparatus as recited in claim 6, wherein said bit is contained within a flags register.
8. (Original) The apparatus as recited in claim 6, wherein said interrupting event comprises a transfer of program control to a program flow configured to process said interrupting event, and wherein execution of said one of the cryptographic operations on a current input text block is interrupted.
9. (Original) The apparatus as recited in claim 8, wherein, upon return of program control to said cryptographic instruction, said one of the cryptographic operations is performed on said current input text block.
10. (Currently Amended) The apparatus as recited in claim 1, wherein said CFB mode logic directs said ~~microprocessor pipeline~~ microprocessor to modify said pointer registers to point to next input and output text blocks at the completion of each of said plurality of CFB block cryptographic operations on each of said corresponding plurality of input text blocks.

11. (Currently Amended) The apparatus as recited in claim 1, wherein said CFB mode logic directs said ~~microprocessor~~pipeline ~~microprocessor~~ to store a current output text block to a memory location pointed to by an initialization vector register.
12. (Previously Presented) The apparatus as recited in claim 6, wherein said interrupting event comprises an interrupt, an exception, a page fault, or a task switch.
13. (Original) The apparatus as recited in claim 1, wherein said cryptographic instruction is prescribed according to the x86 instruction format.
14. (Currently Amended) The apparatus as recited in claim 1, wherein said cryptographic instruction implicitly references a plurality of registers within said ~~microprocessor~~pipeline ~~microprocessor~~.
15. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a first register, wherein contents of said first register comprise a first pointer to a first memory address, said first memory address specifying a first location in memory for access of said plurality of input text blocks upon which said one of the cryptographic operations is to be accomplished.
16. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a second register, wherein contents of said second register comprise a second pointer to a second memory address, said second memory address specifying a second location in said memory for storage of a corresponding plurality of output text blocks, said corresponding plurality of output text blocks being generated as a result of accomplishing said one of the cryptographic operations upon a plurality of input text blocks.

17. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a third register, wherein contents of said third register indicate a number of text blocks within a plurality of input text blocks.
18. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a fourth register, wherein contents of said fourth register comprise a third pointer to a third memory address, said third memory address specifying a third location in memory for access of cryptographic key data for use in accomplishing said one of the cryptographic operations.
19. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a fifth register, wherein contents of said fifth register comprise a fourth pointer to a fourth memory address, said fourth memory address specifying a fourth location in memory for access of an initialization vector for use in accomplishing said one of the cryptographic operations.
20. (Original) The apparatus as recited in claim 14, wherein said plurality of registers comprises:
a sixth register, wherein contents of said sixth register comprise a fifth pointer to a fifth memory address, said fifth memory address specifying a fifth location in memory for access of a control word for use in accomplishing said one of the cryptographic operations, wherein said control word prescribes cryptographic parameters for said one of the cryptographic operations.

21. (Original) The apparatus as recited in claim 1, wherein said execution logic comprises:

a cryptography unit, configured to execute a plurality of cryptographic rounds on each of said plurality of input text blocks to generate a corresponding each of a plurality of output text blocks, wherein said plurality of cryptographic rounds are prescribed by a control word that is provided to said cryptography unit.
22. (Currently Amended) An apparatus for performing cryptographic operations, comprising:

a cryptography unit disposed within a ~~microprocessor~~ pipeline microprocessor, configured to execute one of the cryptographic operations responsive to receipt of a cryptographic instruction within an ~~instruction flow~~ application program that prescribes said one of the cryptographic operations, wherein said one of the cryptographic operations comprises:

plurality of CFB block cryptographic operations performed on a corresponding plurality of input text blocks; and

CFB mode logic, operatively coupled to said cryptography unit, configured to direct said ~~microprocessor~~ pipeline microprocessor to update pointer registers and intermediate results for each of said plurality of CFB block cryptographic operations.
23. (Original) The apparatus as recited in claim 22, wherein an interrupting event causes a transfer of program control to a program flow configured to process said interrupting event, and wherein execution of said one of the cryptographic operations on a current input text block is interrupted.
24. (Original) The apparatus as recited in claim 23, wherein, upon return of program control to said cryptographic instruction, said one of the cryptographic operations is performed on said current input text block.

25. (Currently Amended) The apparatus as recited in claim 22, wherein said CFB mode logic directs said ~~computing microprocessor~~pipeline ~~microprocessor~~ to modify said pointer registers to point to next input and output text blocks at the completion of each of said plurality of CFB block cryptographic operations on each of said corresponding plurality of input text blocks.
26. (Currently Amended) The apparatus as recited in claim 22, wherein said CFB mode logic directs said ~~computing microprocessor~~pipeline ~~microprocessor~~ to store a current output text block to a memory location pointed to by an initialization vector register.
27. (Original) The apparatus as recited in claim 22, wherein said cryptographic instruction is prescribed according to the x86 instruction format.
28. (Currently Amended) A method for performing cryptographic operations in a device, the method comprising:

via a cryptography unit within a ~~microprocessor~~pipeline ~~microprocessor~~,
executing one of the cryptographic operations responsive to receiving a cryptographic instruction, wherein the cryptographic instruction prescribes the one of the cryptographic operations, said executing comprising:

performing a plurality of CFB mode block operations on a corresponding plurality of input text blocks; and

writing a current input text block to an initialization vector location so that a following one of the plurality of CFB mode block operations on a following one of the plurality of input text blocks will employ the current input text block as an initialization vector equivalent.
29. (Original) The method as recited in claim 28, further comprising:

transferring program control to a program flow configured to process a interrupting event, and interrupting said executing of the one of the cryptographic operations on the current input text block.

30. (Original) The method as recited in claim 29, further comprising:
upon return of program control to the cryptographic instruction following said
transferring, performing said executing on the current input text block.
31. (Original) The apparatus as recited in claim 28, wherein said receiving comprises:
prescribing the cryptographic instruction according to the x86 instruction format.
32. (Original) The method as recited in claim 28, wherein said receiving comprises:
prescribing a cipher feedback mode decryption operation as the one of the
cryptographic operations.
33. (Original) The method as recited in claim 28, wherein said executing comprises:
accomplishing the one of the cryptographic operations according to the Advanced
Encryption Standard (AES) algorithm.
34. (Original) The method as recited in claim 28, wherein said receiving comprises:
specifying, within the cryptographic instruction, a cipher feedback mode to be
employed in accomplishing the one of the cryptographic operations.